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Attorney Docket No. FUJ 00-01013RAM
Client Matter No. 80458.0007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	09/742,204	Confirmation No. 7135	
Inventors:	Glen FOX, et al.	Title:	PROCESS FOR PRODUCING HIGH QUALITY PZT FILMS FOR FERROELECTRIC MEMORY INTEGRATED CIRCUITS
Filed:	December 20, 2000		
TC/A.U.	2823		
Examiner:	W. David COLEMAN		
Docket No.	FUJ 00-01013RAM		
Customer No.	25235		

APPEAL BRIEF

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal was filed with the U.S. Patent & Trademark Office on August 13, 2004 in the above case, appealing from a Final Office Action mailed April 21, 2004, rejecting all claims 1-10, 12, 14-17, 19, 20, 22, 24 and 27. This Appeal Brief filed by Express Mail on October 13, 2004, is thus timely filed.

I. REAL PARTY IN INTEREST

The real party in interest is Fujitsu Limited to which the inventors have assigned all rights in U.S. Serial No. 09/742,204 in an Assignment recorded at Reel/Frame Nos. 011920/0967 in the U.S. Patent & Trademark Office.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-10, 12, 14-17, 19, 20, 22, 24 and 27 are presented, with the rejection of claims 1-10, 12, 14-17, 19, 20, 22, 24 and 27 is appealed herein. No claims are cancelled herein.

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IV. STATUS OF AMENDMENTS

No amendments are pending.

V. SUMMARY OF THE INVENTION

According to the present invention as claimed, a perovskite phase can be obtained through a first anneal and, thereafter, a top electrode layer covering the layer of ferroelectric dielectric material is formed. Top electrode formation is followed by a second anneal. Through the second anneal, crystallization of the layer of ferroelectric dielectric material can be completed. The second anneal is performed by rapid thermal annealing, and a second annealing temperature is adjusted higher than the first annealing temperature. The invention as claimed provides improved ferroelectric performance, and highly integrated ferroelectric capacitors having excellent performance characteristics can be obtained.

VI. ISSUES

A. Whether Claims 1-10 and 27 are Patentable Under 35 U.S.C. § 103(a) over U.S. Patent No. 6,682,772 to *Fox* in view of *Mochizuki* (U.S. Patent No. 6,190,957).

B. Whether Claims 12, 14-17, 19, 20, 22 and 24 are Patentable Under 35 U.S.C. § 103(a) over *Fox* in view of *Mochizuki*.

VII. GROUPING OF CLAIMS

Claims 1-10 and 27 are grouped together herein. Claims 12, 14-17, 19, 20, 22 and 24 are grouped together herein.

VIII. ARGUMENT

A. Rejection of Claims 1-10 and 27 over *Fox* in view of *Mochizuki*.

1. There is no motivation to combine *Fox* and *Mochizuki* sufficient to support an obviousness rejection of claims 1-10 and 27.

2. Even if combinable, *Fox* and *Mochizuki* together fail to teach all of the recited limitations of claims 1-10 and 27.

3. A rejection based upon a combination of elements from *Fox* and *Mochizuki* results from a hindsight combination using claims 1-10 and 27 as a roadmap.

B. Rejection of Claims 12, 14-17, 19, 20, 22 and 24 over *Fox* in view of *Mochizuki.*

1. There is no motivation to combine *Fox* and *Mochizuki* sufficient to support an obviousness rejection of claims 12, 14-17, 19, 20, 22 and 24.

2. The rejection of claims 12, 14-17, 19, 20, 22 and 24 is an impermissible combination of features from *Fox* and *Mochizuki* arbitrarily combined using hindsight.

A(1) There is no motivation to combine *Fox* and *Mochizuki* sufficient to support an obviousness rejection of claims 1-10 and 27.

Fox teaches that a first anneal (500 to 650 °C) and a second anneal (700 to 750 °C) are performed after forming a PZT layer on a bottom electrode. The PZT layer is crystallized after the two anneals are formed in an additional step. Thereafter, the top electrode is formed.

Mochizuki teaches formation of a bottom electrode and ferroelectric layer followed by a rapid thermal anneal (RTA anneal) at 800 °C, formation of a top electrode, and then a conventional anneal at 600 °C.

The rejection of claims 1-10 and 27 under 35 U.S.C. § 103(a) is respectfully traversed because there is no motivation to combine the teachings of *Fox* and *Mochizuki.*

The patent statue provides that "[a] patent may not be obtained ... if the differences between the [claimed invention] and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a) (Supp. III 1997) (emphasis added). In establishing non-obviousness the Federal Circuit has ruled that hindsight reconstruction, and specifically the "pick and choose" method of hindsight reconstruction is expressly forbidden in a "103" non-obviousness analysis. One "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 837 F.2d 1071, 1075 (Fed.Cir.1988) (emphasis added).

To counter a charge of hindsight-based obviousness analysis there must be a rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references. *See In re*

Dembiczak, 175 F.3d at 999 (Fed.Cir.1999) ("Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight.")

Having a motivation to combine the references is thus fundamental to sustaining a non-obviousness-type rejection. "When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references." *In re Rouffet*, 149 F.3d 1350, 1355 (Fed.Cir.1998) (*citing In re Geiger*, 815 F.2d 686, 688 (Fed.Cir.1987)). "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577 (Fed.Cir.1984).

Therefore, "[w]hen determining the patentability of a claimed invention which combines two known elements, 'the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.' " *In re Beattie*, 974 F.2d 1309, 1311-12 (Fed.Cir.1992) (quoting *Lindemann*, 730 F.2d at 1462 (emphasis added).

The requirement for a motivation to combine the references is especially pertinent in chemical and semiconductor process inventions due to the unpredictability of the results in varying the process components and conditions even by a small amount or exchanging and re-combining processing steps. *See In re Kerkoven*, 626 F.2d 846 (U.S. Ct. of Customs & Patent Appeals 1980) (Noting the "uncertainty and unpredictability often associated with the chemical arts".)

Fox and *Mochizuki* both teach "stand alone" methods for providing a ferroelectric capacitor. The method taught by *Fox* chooses to provide a first anneal and a second anneal between the formation of the ferroelectric layer and formation of the top electrode. There is no suggestion of desirability in *Fox* to split up the two anneals, with a first anneal performed between the formation of the ferroelectric layer and the formation of the top electrode layer, and with a second anneal performed after a top electrode is formed.

Similarly, *Mochizuki* chooses to provide an RTA anneal between the formation of the ferroelectric layer and the top electrode layer. A second anneal at a temperature lower than the first temperature is then performed after formation of the top electrode layer. There is no suggestion of desirability in *Mochizuki* relative to the anneals or temperature protocol developed by *Fox*. Rather the precise technique taught by *Mochizuki* involving an RTA anneal and specified annealing temperatures are tailored to provide optimum performance for the *Mochizuki* method as taught.

In the Advisory Action, the motivation for combining the teachings of *Fox* and *Mochizuki* is that the "references are combinable to yield the Applicants' claimed invention in order to prevent deterioration in the characteristics of a ferroelectric capacitor and enabling process integration when a ferroelectric memory is manufactured", citing column 6, lines 14-21 of *Mochizuki*. This is another way of stating that because the "references are combinable", they should be combined. That is no motivation at all.

The Examiner's rationale and citation from *Mochizuki* fall short of an adequate motivation for combining the *Fox* and *Mochizuki* references. The entire *Mochizuki* citation follows:

> An object of the present invention is to provide a method of manufacturing a semiconductor apparatus capable of preventing deterioration in the characteristics of a ferroelectric capacitor and enabling process integration when a ferroelectric memory cell is manufactured, and a semiconductor apparatus manufactured by the method according to the present invention.

This citation is merely a general statement of intent to provide a semiconductor process method for producing a ferroelectric capacitor. It does not include any motivation to use the switching the anneal protocol of *Mochizuki*, other than it is applicable to ferroelectric capacitor manufacturing generally. The Examiner has not pointed to language in either *Fox* or *Mochizuki* that contains a specific suggestion that the anneal protocols could be changed, or the anneal temperatures inverted, or any other similar suggestion for combining one reference with the other.

A(2) A combination of *Fox* and *Mochizuki* with *Fox* as the primary reference fails to teach all of the recited limitations of claim 1-10 and 27

If the teachings of *Fox* and *Mochizuki* are arbitrarily combined as in the Office Action, the method of the present invention as claimed does not necessarily result.

Using *Fox* as the primary reference in combination with the teachings of *Mochizuki*, the following method of forming a ferroelectric capacitor results: forming a bottom electrode layer, forming a ferroelectric layer, performing a first RTA anneal at 800 °C, performing a second anneal at 600 °C, and then forming a top electrode layer. This hypothesized combination method differs from the method claimed in the present invention. Claims 1 and 27 recite a first anneal temperature which is lower and a second anneal temperature which is higher. Also, claims 1 and 27 recite a split anneal process: a first anneal—then top electrode deposition—then a second anneal. The combination. *Fox* modified by *Mochizuki* involves a first anneal—then a second anneal which is a rapid thermal anneal—then top electrode deposition. Claims 1 and 27 are patentably distinguishable over this combination, as are claims 2-10 depending from claim 1.

A(3) The rejection of claims 1-10 and 27 is an impermissible combination of features from *Fox* and *Mochizuki* arbitrarily combined using hindsight.

It should be understood that both references are "stand alone" recipes for creating ferroelectric capacitors. They are not just catalogues of various processing steps that can be separated out and used as desired to deny the patentability of novel and non-obvious claimed inventions. The unpredictability of the chemical arts is the essential reason why this "pick and choose" technique is not used in semiconductor manufacturing. Successful new semiconductor processing recipes are usually perfected after much experimentation and trial wafer runs.

Put another way, what is essentially improper about the way that *Fox* and *Mochizuki* are combined in the rejection of claims 1 and 27, is that an arbitrary combination of features are used—a technique involving the picking and choosing of features with hindsight gleaned from the claimed methodology:

> Start with *Fox*—then unlike *Fox*, split the anneals, forming the top electrode between the first and second anneals—then unlike *Fox*, make the second anneal a rapid thermal anneal—but keep the relative anneal temperatures described in *Fox*, with the 2nd anneal at a higher temperature than the 1st anneal.

Using the two references in this manner to selectively choose features of each using the present invention as a roadmap is a technique expressly prohibited by the Federal Circuit. For this additional reason, claims 1-10 and 27 are patentable over the combination of *Fox* and *Mochizuki*.

B(1) There is no motivation to combine *Fox* and *Mochizuki* sufficient to support an obviousness rejection of claims 12, 14-17, 19, 20, 22 and 24.

As discussed above in connection with claims 1-10 and 27, the Examiner's rationale and citation from *Mochizuki* fall short of an adequate motivation for combining *Fox* and *Mochizuki*. The citation relied upon is merely a general statement of intent to provide a semiconductor process method producing a ferroelectric capacitor. It does not include any motivation to use the split anneal protocol of *Mochizuki*, other than it is applicable to ferroelectric capacitor manufacturing generally. The Examiner has not pointed to language in either *Fox* or *Mochizuki* containing a specific suggestion regarding the desirability of changing the anneal protocols or any other similar suggestion for combining one reference with the other. This argument applies equally to the lack of motivation for combining the references with respect to dependent claims 12, 14-17, 19, 20, 22 and 24.

B(2) The rejection of claims 12, 14-17, 19, 20, 22 and 24 is an impermissible combination of features from *Fox* and *Mochizuki* Arbitrarily Combined Using Hindsight.

As discussed in detail above with respect to the rejection of claims 1-10 and 27, both references are "stand alone" very specific recipes of chemical constituents and manufacturing conditions for creating ferroelectric capacitors. They are not just catalogues of various processing steps that can be separated out and used as desired to deny the patentability of novel and non-obvious claimed inventions. The unpredictability of the chemical arts is the essential reason why this "pick and choose" technique is not used in semiconductor manufacturing.

Successful new semiconductor processing recipes are usually perfected after much experimentation and trial wafer runs.

Put another way, what is essentially improper about the way that *Fox* and *Mochizuki* are combined in the rejection of claim 12 and the claims that depend therefrom, is that an arbitrary combination of features are used—a technique involving the picking and choosing of features with hindsight gleaned from the claimed methodology:

> Start with *Fox*—then unlike *Fox*, split the anneals, forming the top electrode between the first and second anneals—then unlike *Fox*, make the second anneal a rapid thermal anneal—but keep the relative anneal temperatures described in *Fox*, with the 2nd anneal at a higher temperature than the 1st anneal.

Using the two references in this manner to selectively choose features of each using the present invention as a roadmap is a technique expressly prohibited by the Federal Circuit. For this additional reason, claims 12, 14-17, 19, 20, 22 and 24 are patentable over the combination of *Fox* and *Mochizuki*.

IX. Conclusion.

For the reasons given above, claims 1-10, 12, 14-17, 19, 20, 22, 24 and 27 are non-obvious over the combination of references cited. Overruling the rejections of these claims is thus respectfully requested.

Please charge Deposit Account No. 50-1123 the $330.00 large entity fee associated herewith and any other fee required for this filing.

Respectfully submitted,

October 13, 2004

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X. APPENDIX

1. (Previously presented) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising:

deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal at a first temperature;

deposition of an electrically conductive top electrode layer; and

annealing the layer of ferroelectric dielectric material with a second anneal at a second temperature higher than the first temperature, the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer.

2. (Original) The process of Claim 1, wherein the electrically conductive bottom electrode layer comprises a noble metal.

3. (Original) The process of Claim 2, wherein the electrically conductive bottom electrode layer comprises platinum.

4. (Original) The process of Claim 1, wherein the ferroelectric dielectric layer comprises PZT.

5. (Original) The process of Claim 1 wherein the electrically conductive top electrode layer comprises a noble metal oxide.

6. (Original) The process of Claim 5 wherein the electrically conductive top electrode layer comprises Iridium Oxide.

7. (Original) The process of Claim 5 wherein the first anneal comprises a rapid thermal anneal at a temperature between five hundred twenty five and six hundred degrees celsius.

8. (Previously Presented) The process of Claim 1, wherein the first anneal is performed by rapid thermal annealing.

9. (Original) The process of Claim 7 wherein the second anneal is performed at a temperature of between seven hundred and seven hundred fifty degrees celsius.

10. (Original) The process of Claim 9, wherein the second anneal is performed at a temperature of approximately seven hundred twenty five degrees celsius for a duration of greater than ten seconds.

11. (Canceled)

12. (Previously presented) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising:

deposition of an electrically conductive bottom electrode layer comprising a noble metal;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal in an environment comprising oxygen at a first partial pressure;

deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed in an environment comprising oxygen, the oxygen having a second partial pressure less than the first partial pressure and performed after the step of deposition of an electrically conductive top electrode layer.

13. (Canceled)

14. (Previously presented) The process of Claim 12, wherein the second anneal is performed by rapid thermal annealing.

15. (Previously presented) The process of Claim 12 wherein the first partial pressure is less than ten percent of one atmosphere.

16. (Previously presented) The process of Claim 12 wherein the first anneal is performed by rapid thermal annealing.

17. (Previously presented) The process of Claim 12 wherein the second anneal is performed in an environment comprising a mixture of oxygen and inert gas.

18. (Canceled)

19. (Previously presented) The process of Claim 12 wherein the second partial pressure is less than five percent of one atmosphere.

20. (Previously presented) The process of Claim 12 wherein the first anneal is performed in an environment comprising a mixture of oxygen and inert gas.

21. (Canceled)

22. (Previously presented) The process of Claim 12 wherein the second anneal is performed at a temperature of between seven hundred and seven hundred fifty degrees celsius for a time not less than ten seconds.

23. (Canceled)

24. (Previously presented) The process of Claim 12 wherein the step of depositing the ferroelectric dielectric layer is performed by sputtering.

Claims 25 - 26. (Canceled)

27. (Previously presented) A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising:

deposition of an electrically conductive bottom electrode layer comprising a noble metal;

deposition of a layer of ferroelectric dielectric material by a sputtering method;

annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal at a first temperature;

deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal at a second temperature higher than the first temperature, the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed by rapid thermal annealing after the step of deposition of an electrically conductive top electrode layer.

Claims 28 - 31 (Canceled)

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October 13, 2004

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